REMARKS/ARGUMENTS

Reconsideration of this application as amended is respectfully requested.

Claims 1-4, 12-15, 22 and 23 remain pending in this application.

Claims 1, 2 and 4 stand rejected under 35 USC 102 as being anticipated by U.S. Patent No. 5,802,132 (Pathikonda); claims 3, 12 and 13 stand rejected under 35 USC 103 as being unpatentable over Pathikonda, in view of, U.S. Patent No. 5,329,471 (Swoboda); and claims 14, 15, 22 and 23 stand rejected under 35 USC 103 as being unpatentable over Pathikonda, in view of, U.S. Patent No. 5,471,587 (Fernando). Applicant respectfully traverses.

According to the Examiner, with respect to claim 1, Pathikonda discloses an integrated circuit comprising at least three cooperating frequency domains having variable operating frequencies (fig. 6B; col. 8, lines 39-54), wherein the at least three domains each operate at different frequencies (fig. 6A; col. 8, lines 13-30); the Examiner further states that since claim 12 is written in means plus function format and contains the same limitation as 1, the same rejection applies. In addition, the Examiner, with respect to claim 22, discloses that Pathikonda teaches at least the first, second, and third portions each operate at different frequencies; the Examiner further states that since claim 14 is written in means plus function format and contains the same limitations as claim 22, the same rejection applies. Applicant respectfully disagrees.

Pathikonda teaches a core clock domain which is clocked by a core clock signal, a bus clock domain logic which is clocked by a bus clock signal. Interfacing the bus clock domain logic to the core clock domain logic is the bus clock prime domain logic. The bus clock prime domain logic is clocked by a bus clock prime signal. Pathikonda further teaches that the signals between the bus clock prime domain and the core clock domain may cross over easily because the core clock signal and the bus clock prime signal are always aligned (emphasis added) (See col. 8, lines 13-54 and col. 13, lines 36-40).

Applicant argues that nowhere does Pathikonda teach or disclose three domains where each domain operates at a different frequency. Rather, in Pathikonda, the bus clock prime signal (for one domain) and the core clock signal (for a second domain) are said to be always aligned as opposed to operating at different frequencies. Thus, the prior art

operates, at most, in only two frequencies rather than three frequencies. Therefore, Pathikonda fails to teach or disclose at least three domains where each domain is operating at a different frequency.

In summary, for the reasons noted above, Claims 1-4, 12-15, 22 and 23 are distinguished over the cited art and are in condition for allowance. It is respectfully submitted that in view of the arguments set forth herein, the applicable rejections have been overcome. Favorable action is respectfully solicited. Allowance of the Claims is respectfully requested.

Please charge any additional charges to our Deposit Account No. 02-2666.

Respectfully submitted,

BLAKELY, SOKOLOFF, TAYLOR & ZAFMAN LLP

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John Patrick Ward
Reg. No. 40,216

12400 Wilshire Blvd.
Seventh Floor
Los Angeles, CA 90025
(408) 720-8300